**DCS Lab **

**Experiment - 5**

**Aim:** Implement 4 bit ripple carry adder using structural modeling. Implement 4 bit adder/subtractor using structural modeling.

Description:

1. Use structural modeling to implement a 4 bit adder to add two 4 bit vectors A and B with initial carry Cin and output sum vector S with output carry bit Cout. Use full adder as a component. Verify the results using testbench

Show your output by taking the following input cases.

9+ 3

7 + 6

9 + A

1 + F

1. Use structural modeling to implement a 4 bit adder/ subtractor to add/subtract two 4 bit vectors A and B with Control input as M. Output sum vector S with output carry bit Cout. Use full adders as components. Verify the results using testbench.

Show your output by taking the following input cases.

M = 0, A = 5 B = 9

M = 1 A = + 5 and B = + 3

M =1 A = + 3 and B = + 5

Part2:

For each type of the above implementations generate the synthesis report.

Study delay and cell usage for both Adder as well as adder/subtractor.